

Figure 1

		210a	210b	210n	
		Order 1	Order 2		Order n
220a	Token 1	1	1	1	0
220b	Token 2	1	0	0	1
220c	Token 3	1	1	0	1
220n	Token n	0	1	1	0

200

Figure 2

		310a	310b	310n	
		Order 1	Order 2		Order n
320a	Restriction 1	0	0	1	0
320b	Restriction 2	0	1	0	1
320c	Restriction 3	1	0	0	1
320n	Restriction n	1	1	1	0

300

Figure 3

		410a	410b	410n	
		Period 1	Period 2		Period n
420a	Restriction 1	12	6	0	19
430a	Vector 1	1	1	0	1
420b	Restriction 2	0	0	2	23
430b	Vector 2	0	0	1	1
420n	Restriction n	0	0	6	2
430n	Vector n	0	0	1	1

Figure 4

		510a	510b	510n	
		Period 1	Period 2		Period n
520a	Pointer to Restriction1	12	6	0	19
530a	Pointer to Vector 1	1	1	0	1
520b	Pointer to Restriction2	0	0	2	23
530b	Pointer to Vector 2	0	0	1	1
540	Result Vector	0	0	0	1

Figure 5

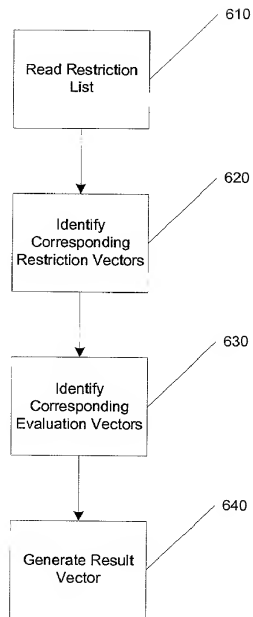


Figure 6

		710a	710b	710n	
		Order 1	Order 2		Order n
720a	Item 1/EN1	1	1	0	0
720b	Item 1/EN2	0	0	1	1
720c	Item 2	1	0	0	1
720n	Item n	1	0	1	0

Figure 7

	Order 1	Order 2		Order n
Item 1/EN1	1	1	0	0
Item 1/EN2	0	0	1	1
Item 2	1	1	1	1
Item n/EN1	1	1	0	0
Item n/EN2	0	0	1	1

Figure 8

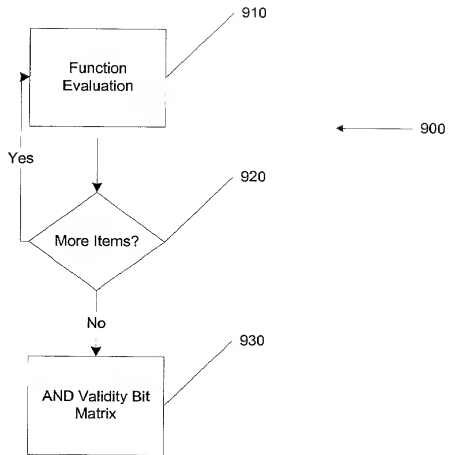


Figure 9

1010

Restrict.	Effectivity	Selection Condition
R_1	EN_1	C_1='V_1'
R_1	EN_2	C_1='V_2'

1020

Eff. Number	Validity
EN_1	1/1/2000
EN_2	7/1/2000

1030

	Order 1	Order 2	Order 3
C_1='V_1'	1	0	1
C_1='V_2'	0	1	1

Explode

1040

	Order 1	Order 2	Order 3
R_1/EN_1	1	0	1
R_1/EN_2	0	1	1

	6/28	6/29	6/30	7/1	7/2	7/3
Restriction 1	0	3	1	0	3	4
Bit	0	1	1	0	1	1

1050

EN_1	1	1	1
EN_2	0	0	0

0	0	0
1	1	1

1060

Order 1	0	1	1
Order 2	1	1	1
Order 3	0	1	1

1	1	1
0	1	1
0	1	1

1070

Figure 10

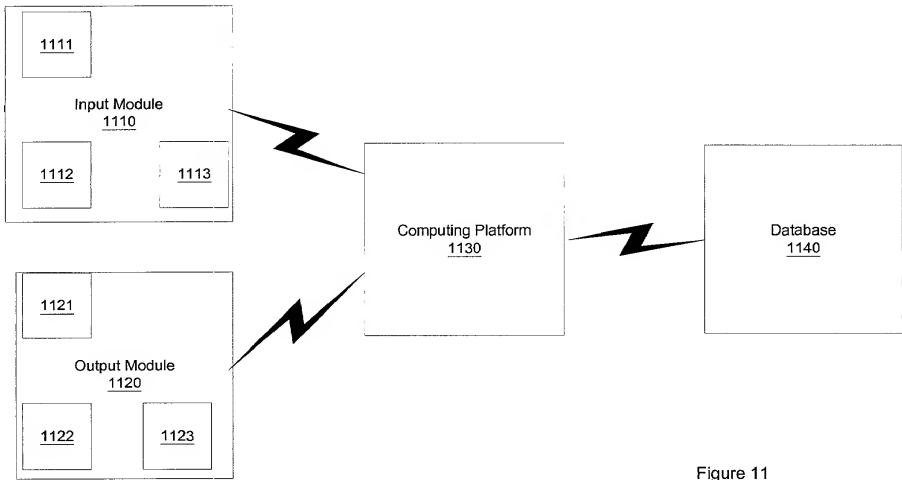


Figure 11